REMARKS

Claims 1-20 are pending in this application. Claims 12, 15 and 16 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections while Claims 17-20 have been newly added in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

Claims 1-11, 13 and 14 have been allowed without the necessity of amendments. The Examiner's indication of allowability of these claims is noted with appreciation.

The title of the invention has been objected for failing to be sufficiently descriptive. Accordingly, a new title of –Power Converter Using A Semiconductor Switching Device— is hereby submitted for the Examiner's consideration and entry.

Remaining claims 12, 15 and 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Koichi, JP 7170723 for reasons stated on pages 2-4 of the Office Action (Paper No. 6). For purposes of expedition, claims 12, 15 and 16 have been amended to further define Applicants' disclosed invention and to distinguish over the cited prior art, including Koichi, JP 7170723, so as to render the rejection moot. For example, base claims 12 and 15 have been amended to define that "respective junction between each of said first and second control signal lines and the circuit portion of said semiconductor circuit is **covered by** selected one of an area of said main circuit wiring where said main circuit current flows and said plurality of said tabular conductors are in superposed relation to each other and an area of said main circuit wiring where said main circuit current does not flow" and

"that portion of each of said first and second control signal lines which is **cover d by** one of said tabular conductors with said main circuit current flowing therein".

As shown in FIG. 2, as attached as EXHIBIT A, the junction or the branch point of the control signal line 82 and the junctions or the gate terminals to which the gate signal lines 822A and 822B are connected are **covered by** the tabular conductor shown with a dotted line.

Base claim 16 has been amended to further define that "said control signal line crosses **in the vicinity of** an end of an area of said main circuit wiring where said main circuit current flows and said plurality of said tabular conductors are in superposed relation to each other, between the side of said main circuit wiring where said semiconductor switching device is located and the opposite side of said main circuit wiring". Such a "control signal line passes in the vicinity of an end portion of the main circuit wiring" is described on page 5, lines 1-3 of Applicants' specification.

As amended, claims 12, 15 and 16 are believed to be allowable over Koichi, JP 7170723. However, to the extent that the rejection may still be applicable, Applicants respectfully traverse the rejection for the reasons discussed herein below.

As previously discussed, base claim 12 requires that the "respective junction between each of said first and second control signal lines and the circuit portion of the semiconductor circuit is **covered by** selected one of an area of said main circuit wiring ..."

Likewise, base claim 15 requires that "each of the junction between said control lines and the circuit portion of said semiconductor circuit is **covered by** selected one of an area of said main circuit wiring ..."

Base claim 16 requires that the "control signal line crosses **in the vicinity of** an end of an area of said main circuit wiring where said main circuit current flows and said plurality of said tabular conductors are in superposed relation to each other, between the side of said main circuit wiring where said semiconductor switching device is located and the opposite side of said main circuit wiring".

In contrast to Applicants' base claims 12 and 15, Koichi '723 discloses a completely different semiconductor stack as shown in FIG. 1, in which the control signal lines 14 and the connection points 15, 17 and 18 of the control signal lines 14 and the circuit **are located outside** the tabular conductor 27. In other words, the control signal lines 14 and the connection points 15, 17 and 18 are **not** covered by the tabular conductor 27.

In addition, in contrast to Applicants' base claim 16, Koichi '723 discloses that the control signal lines 14 are apart from the edge of the tabular conductor.

The rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

The burden of establishing a basis for denying patentability of a claimed invention rests upon the Examiner. The limitations required by the claims cannot be ignored. See In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). All claim limitations, including those which are functional, must be considered. See In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981). Hence, all words in a claim must be considered in deciding the patentability of that claim against the prior art. Each word in a claim must be given its proper meaning, as construed by a person skilled in the art. Where required to determine the scope of a recited term, the disclosure may be used. See In re Barr, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

In the present situation, Koichi '723 fails to disclose and suggest key features of Applicants' claims 12, 15 and 16. Therefore, Applicants respectfully request that the rejection of claims 12, 15 and 16 be withdrawn.

Claims 17-20 have been newly added to alternatively define Applicants' disclosed invention over the prior art of record. These claims are believed to be allowable at least for the same reasons discussed against all the outstanding rejections of the instant application. In addition, claim 17 further defines that "even at a place in the vicinity of said end which is otherwise easily affected by said main circuit current, the effect of said main circuit current on said control signal line is relaxed" as described on page 1, lines 12-18 of Applicants' specification. No where in the cited prior art, including Koichi '723 is there any disclosure or suggestion of features of Applicants' claim 17. Likewise, claims 18-20 capture the features of the allowed claim 1, 13 and 14. As a result, claims 18-20 should also be in condition for allowance. No fee is incurred by the addition of claims 17-20.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 500.41483X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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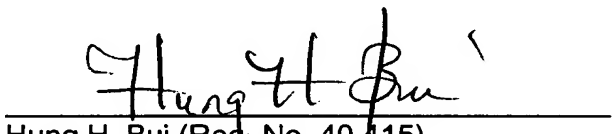
By 

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